prof. Ing. Miloš Drutarovský, CSc.

Department of Electronics and Multimedia
Telecommunications
Faculty of Electrical Engineering and
Informatics
Technical University of Kosice
Nemcovej 32, 042 00 Kosice
Slovak Republic
Tel.: +421 55 602 4362
E-mail: Milos.Drutarovsky@tuke.sk

Doctoral Thesis Review

Reliable FPGA Architecture submitted by Ing. Jan Pospíšil

The thesis has been submitted to the Faculty of Information Technology, Czech Technical University in Prague, in Ph.D. study programme Informatics in August 2018.

Structure of the doctoral thesis

The manuscript text has 98 numbered pages and is divided into 7 chapters, bibliography with 84 items, four lists of author's publications (4 reviewed publications relevant to the thesis A.1-A.4, 7 remaining publications relevant to the thesis A.5-A.11, 6 remaining publications A.12-A.17, and 78 remaining publications (ALICE Collaboration) A.18-A.95), list of 11 author's citations B.1-B.11 and 2 appendixes with an example of place and route results and used implementation scripts. Chapter 1 explains research motivation, problem statement and goals of submitted thesis. Chapter 2 provides basic definitions, terminology and background for Filed Programmable Gate Arrays (FPGAs) architectures and Xilinx design language, radiation effects in CMOS circuits and their testing in the isonchronous cyclotron U-120M at NPI Řež. Chapter 3 summarizes the previous results and related work in the area of commercially available radiation tolerant FPGAs, available results of irradiation tests, and non-commercial FPGA design flow tools used in the thesis. Chapter 4 presents overview of proposed approach how to create and use simulation model for quantitative characterization of FPGA designs in terms of radiation dependability. Chapter 5 describes a proof-of-concept implementation of the proposed method for the Xilinx Spartan-3 FPGA chip family. The results of the proposed model usage tested on several standardized benchmarks are presented and discussed in Chapter 6. Chapter 7 summarizes the results presented in the thesis and suggests themes for the future work.

Relevance of the selected topic and aims of the doctoral thesis

Static RAM (SRAM) based FPGA devices are used in many different fields of electronics for quite long period. The well-known inherent drawback of these devices is their susceptibility also to Single Event Effects (SEEs). The reliability of such devices decreases with radiation induced soft errors in radiation critical applications (e.g. electronics operated on the orbit). The heavy-ion detector on the Large Hadron Collider (LHC) called ALICE (A Large Ion Collider Experiment) is another example application where a lot of SRAM FPGAs are also typically used. Researches form many universities, including those from FIT CTU in Prague, contribute to the development of

ALICE hardware. The design reliability of used FPGAs designs in such applications must be evaluated also for increased radiation conditions. Experimental evaluation of mitigation techniques for such designs could be quite expensive and time consuming. The aim of the doctoral thesis is to develop a method for simulation-based evaluation of radiation induced soft errors, such as Single Event Upset (SEU), in the SRAM based FPGAs by using radiation related parameters obtained form real hardware experiments. Concentration to the efficient evaluation of mitigation techniques of SRAM based FPGA designs is relevant topic in research community. I consider given topic as valuable and sufficient for verification of the originality of the solution in the given filed.

Used methods of the solutions and level of the processing of the doctoral thesis

The submitted thesis offers a solution for simulation-based evaluation of the radiation induced soft error impact to the SRAM based FPGAs. Proposed method uses one-time step of model creation and its calibration followed by repetitive model usage for the digital design simulation. The model uses data (parameters) acquired from experimental radiation tests of real FPGA hardware. The overall failure rate characteristic for an arbitrary digital design implemented on a given FPGA under given environment (radiation) conditions can then be evaluated by using calibrated model of given FPGA.

The doctoral thesis uses standard Xilinx ISE design tool for target Xilinx Spartan-3 FPGA, a set of available non-commercial frameworks and tools for FPGA design flow (Verilog to Routing, RapidSmith, HOPE fault simulator) and own implementation script codes (included in the Appendix B) to model Xilinx Spartan-3 FPGA family. A proof of concept implementation of the proposed method was demonstrated by using these building blocks. The model was calibrated by using experimental measurement data from irradiation accelerated life testing by using cyclotron at Nuclear Physics Institute at Řež.

The tested design is extended by using fault models (based on saboteur concept) and the transformed circuit description is then fault simulated. If real test vectors are supplied for the simulation, the real failure probability of the design in question can be calculated.

The results of proposed method is presented on several benchmarks from Politecnico di Torino subset of ICT99 ones. Results for reduced designs used in irradiation tests are also provided. Some problems with HOPE simulator exception were detected for presented simulations and some reduced simulations were described and executed. Results are provided in the form of tabulated values of reduced observable faults (failure rate) for selected tested designs.

The structure of submitted thesis is balanced and quite well readable, it contains all relevant information in a compact form. It contains only a small number of typographic errors (e.g. ... It is build up from $n_i \times 1$ bit memory on page 9, should be $2\text{^}n_i \times 1$), some statements are not correct, e.g. the statement about MOSFET transistor speed on page 5: "*Basic element of CMOS is Metal-Oxide-Semiconductor field effect transistor (MOSFET, or simply MOS). By simple description, a current flowing through this transistor is directly controlled by the voltage applied in the transistor structure. This difference from BJT (where main current is controlled by current too) offers lower power consumption (because of lack of controlling current) and* ***higher achievable frequencies****, because parasitic capacitances in the control structure doesn't need to be (de)charged by the control current.*".

Author's citations reported on pages 85 and 86 include publication B.1, B.2 and B.8 that are, in my opinion, auto-citations of your co-author T. Vanat. Probably they should not be included.

Original scientific contributions of the doctoral thesis and accomplishment of the stated aims

The thesis presents a new method for simulation-based evaluation of radiation induced soft errors in the SRAM-based FPGA configuration memory based on parameters obtained from

experiments on the real hardware. The method was demonstrated by proof of concept toolchain implementation for chosen Xilinx FPGA family. The proposed method can quickly evaluate the overall failure rate characteristic for an arbitrary digital design implemented on a given FPGA family. Although the target FPGA family (Xilinx Spartan-3) is outdated and the proposed method cannot be easily extended to the modern FPGA families (lack of available design information about included modern blocks, e.g. DSP blocks, no publicly available efficient tools, ...), the proposed results demonstrate a possible approach how radiation induced errors can be evaluated and compared by using modern simulation approach. This is, in my opinion, the main thesis contribution. I appreciate also author's contribution to application of FPGA circuits in the ALICE and LHC projects (mainly publications A.1, A.2, A.12, but also general ALICE collaboration publications). Based on all these facts I consider the aims of the doctoral thesis fulfilled.

Comments and questions

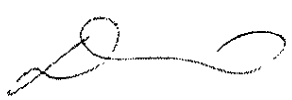
Author presents main benchmark tests in the form of Table 6.4. It contains results in the form of device cross-section (design failure rate) for subset of ITC99 benchmarks. These numbers cannot be checked or confirmed easily. One of the applications of these results could be fast testing of some well-known mitigation techniques (e.g. Triple Module Redundancy, ...) to overcome susceptibility of SRAM FPGAs to e.g. the SEU. Did you try to compare design failure rate of some standard (not protected) design with the protected counterpart? It is a pity such case study comparison results is not included in your thesis. Can you present some simple case study comparison results during thesis defense?

Main results of your thesis were not published at the time of thesis submission. Were these results already published or at least submitted somewhere? Or have been some results of your method already used for some optimization of some, say practical, FPGA based designs?

Table 6.2 on page 60 contains numbers of generated faults for individual fault category and also the overall sum is displayed. The sum for *b02* and *irrad* designs is larger than the actual sum of individual faults. Can you explain why?

Conclusions

The submitted thesis of Ing. Jan Pospíšil addresses important and practical problem of efficient simulation-based evaluation of radiation induced soft errors in the SRAM FPGAs based on parameters obtained form radiation experiments on real FPGA hardware. The author of the thesis in my opinion **proved** by presented thesis and FPGA based research work related to the ALICE project the ability to perform research and achieve scientific results. I **do recommend** the thesis for presentation and defense with the aim of receiving the Degree of Ph.D.



Košice, March 31, 2019

Miloš Drutarovský
reviewer

POLITECNICO DI TORINO

Prof. Luca Sterpone
Dipartimento di Automatica e Informatica, Politecnico di Torino
Corso Duca degli Abruzzi, 24 – 10129 Torino – ITALIA
Phone: +39 011 090 7009 fax: +39 011 090 7099
e-mail: luca.sterpone@polito.it

Torino, 30 March 2019

Subject: Ing. Jan Pospisil - PhD Thesis Evaluation Report

1. **Thesis Title: Reliable FPGA Architecture**
2. **Student Name: Mr. Jan Pospisil**
3. **Supervisor Name: doc. Ing. Jan Schmidt, Ph.D.**
4. **Analysis, observations and general comments** (up-to-dateness, formal structure, completion of the dissertation, assessment and evaluation of the results)

The main goal of the dissertation is to provide reliable simulative models for modern FPGA architecture. The overall structure of the thesis is well composed with a large perspective about the state of the art techniques used for modeling and analyzing radiation effects on different families of FPGAs. However, the background is missing a non-negligible set of references related to simulation and emulation based fault injection that should be included into the dissertation.

The method proposed by the dissertation which is related to the usage of FPGA failure models and architecture sensitivity in order to corrupt by saboteur's simulation processes the behavior of the FPGA is not completely innovative, however the dissertation introduces the concept of "real coverage" and a probability calculation tool that are able to improve the calculation of the error probability.

The description of the method is too short and synthetic. It is not possible to depict from the methodology section, the effective implementation contribution on the explained tools. I strongly recommend to improve this section of the dissertation in order to gain a sufficient technical level.

The experimental validation adopts the traditional ITC benchmarks, a set of circuits largely used on the reliability estimation side. Experimental results and analysis is extremely short and condensed. I strongly encourage the extension of the experimental analysis especially in the part that can be correlated to realistic radiation experiments. At this moment this part of the thesis is not sufficiently extended.

Politecnico di Torino
Corso Duca degli Abruzzi, 24 – 10129 Torino – ITALIA
tel: +39 011 090 7009 fax: +39 011 090 7099
e-mail: luca.sterpone@polito.it

POLITECNICO DI TORINO

Prof. Luca Sterpone
Dipartimento di Automatica e Informatica, Politecnico di Torino
Corso Duca degli Abruzzi, 24 – 10129 Torino – ITALIA
Phone: +39 011 090 7009 fax: +39 011 090 7099
e-mail: luca.sterpone@polito.it

5. Remarks

The dissertation analyses a relevant topic for modern FPGAs, however it has three major critical failings:

1. The methodology is not exposed with sufficient level of details to allow the reader the comprehension of the method. The dissertation includes some basic schemes and nothing else, which is frankly not enough for a PhD dissertation.
2. The experimental analysis is also not extended enough to provide a valuable identification of the improvements provided by the techniques developed by the candidate.
3. Modern FPGAs are today going to 16nm and below, as identified by the dissertation in the background sections. It would be an added value if the candidate extends the experimental analysis with some investigation or comments about the possible application or expected results on such types of devices.

6. Overall evaluation

The overall evaluation of the thesis is not sufficient at the moment. The thesis has interesting points and basics of relevant results. However, the dissertation does not explore them both from the implementation and experimental point of view. Relevant observations should be addressed as aforementioned in the previous section in order to have a sufficient dissertation:

- Improvement of the description of the implemented methodology. More details are necessary.
- Experimental results adding comparative implementation results on more state-of-the-art FPGA families. In cases devices are not available, the candidate can use implementation models available from university program FPGA commercial tools.

7. Final statement

The author of the dissertation proved a sufficient ability to conduct research and achieve scientific results. In accordance with par. 47, letter (4) of the Law Nr. 111/1998 (The Higher Education Act) I do recommend the thesis for the presentation and defense with the aim of receiving the Ph.D. degree upon the integration of the points mentioned in the section 6 of the present evaluation report.

8. Name and Signature of the Examiner
Prof. Luca Sterpone, Department of Computers and Systems Engineering.
Politecnico di Torino, 10129 Torino, Italy

Signature

9. Date of Evaluation
March, 30th 2019

Politecnico di Torino
Corso Duca degli Abruzzi, 24 – 10129 Torino – ITALIA
tel: +39 011 090 7009 fax: +39 011 090 7099
e-mail: luca.sterpone@polito.it

REVIEWER'S REPORT ON PHD DISSERTATION THESIS

"Reliable FPGA Architecture"

Author: Jan Pospisil, Czech Technical University in Prague

The author of the dissertation proposes a simulation-based evaluation of radiation-induced soft errors in SRAM-based FPGAs. The design simulation model includes saboteurs to simulate a fault. Then, these faults are simulated to obtain the fault list of observable faults. Finally, the sensitivity of a circuit is calculated using accelerated radiation testing results for the target FPGA architecture and the list of observable faults.

The dissertation tackles a relevant topic in the area of fault tolerance in reconfigurable architectures. The review of the state-of-the-art presents updated information related to similar works and mitigation techniques for radiation-induced faults.

The organization of the dissertation presents the research topic and the proposal adequately for an external reviewer.

The dissertation fulfills the planned objectives although some remarks are presented in the next paragraphs.

The proposed method is interesting because it could be used to develop more reliable FPGA architectures and evaluate the sensitivity of a design using only the static cross-section of the device.

Although some of the results are partially incomplete due to issues with the selected simulation tool, they are promising. However, a big absence in the result's chapter is a comparison of results obtained from the irradiation test with the results of the proposed method. In particular for the design named 'Irrad'.

I would like to remark that the manuscript should be reviewed to correct several typos and English grammar errors. Also, I have the following questions:

During the assignment of each fault to FPGA resource sensitivity, no mention to the Slice Configuration sensitivity calculated in Table 5.1 is done. Where should be included this resource sensitivity?

Also, a clear explanation of how equation 5.1 was obtained and how the relative' cross-sections of the original paper were used to obtain an absolute cross-section for a specific FPGA resource.

Is it not possible to compare the results obtained for the 'Irrad' design in the irradiation test with the results of the proposed method?

Related to Table 6.4:

Why the observable faults and the reduced observable faults give different results for the design 'b02' if in Table 6.3 'b02' has the same number of undetected faults?

Why the results for all faults and reduced observable faults are different for the design 'Irrad' if the number of reduced undetected faults is zero?

Overall, the thesis is interesting and the proposed method is promising to evaluate future FPGA architectures and designs in the current commercial FPGAs.

Summarizing, the author of the dissertation proved the ability to conduct research and achieve scientific results.

In accordance with par. 47, letter (4) of the Law Nr. 111/1998 (The Higher Education Act) I do recommend the thesis for the presentation and defense with the aim of receiving the Ph.D. degree.

In Graz, Austria, 27.02.2019.

Dr. Ing. Jorge L. Tonfat
jorge.tonfat@oeaw.ac.at
Space Research Institute - OEAW, Graz, Austria