Report from Michel RENOVELL  
Directeur de Recherche CNRS, LIRMM- FRANCE  

On the PhD Dissertation of  
Mr Jiri KVASNICKA  

To receive the degree of Doctor  
From the Czech Technical University in Prague, CZECH REPUBLIC  

The title of the dissertation of Mister Jiri Kvasnicka is:  

«Reliability Analysis of SRAM-based Field-Programmable Gate Arrays»  

The general research work conducted by Mr Kvasnicka analyses the effect of soft errors in the FPGA configuration memory and their consequences on the functionality of the implemented design.  

Today, FPGAs offer a very convenient and cost-effective solution for a lot of applications requiring in-field reprogrammability and applications with small volume productions. However, configuration bits stored into the FPGA configuration memory are prone to soft errors. Indeed, due to technology scaling, the configuration bit vulnerability is becoming a very serious issue. FPGA configuration bit vulnerability is not a new problem. So far, many research works have been dedicated either to configuration bit recovery using some dedicated code mechanisms or to LUT bit protection using classical fault-tolerance techniques. However, there is no work analyzing the relations between a soft error impacting a configuration bit and the corresponding implemented design functional error. In this context, the presented work is very original and innovative.  

The thesis document is divided into 4 main chapters classically embedded between an introduction and a conclusion. Chapter 2 gives the theoretical basis for a better understanding of the whole work. Chapter 3 describes the state of the art in terms of FPGA protection to SEU impact. Chapter 4 presents the original approach and the experimentation that has been implemented in the thesis work. Finally Chapter 5 presents the extensive results obtained from the experimentation.  

Chapter 2 has a clear didactic objective. Basic concepts about digital circuits and logic gate implementation in CMOS technology are reminded. Then, specific structures used in FPGAs are described together with insights on the different FPGA architectures. Finally, a detailed presentation is given about radiation, its definitions, quantities and impacts. The chapter is very clearly written and very didactic, we appreciate the precise definitions and terminology.
Chapter 3 is dedicated to a state of the art of the techniques used in the industry or proposed in the literature for FPGA protection or for error mitigation in standard SRAM-based FPGA. It describes the different hardware hardening solutions used in industrial FPGAs. Some software techniques are also presented such as readback and configuration scrubbing. Finally, design oriented strategies such as the classical triplication are mentioned. This chapter is quite short but still important because it allows to clearly define the positioning of the presented research work in the international context.

In chapter 4 the fundamental contribution of the thesis work is given from a conceptual perspective, i.e. the whole research strategy is presented. The global aim is to contribute to a deep understanding of the SEU effect in the configuration memory and its impact on the implemented combinational circuit. In the first part, faults are classified (class A, B, C and D) according to their output effect (correct or incorrect) but also on the fact that the output is a valid codeword or not. Obviously, the late point is very important when a code checker is used. The second part lists the different FPGA resources that can be impacted by the faults. From my point of view, the third part is very fundamental because fault categories are defined and they will late on be associated with the above fault classes. Finally, the fourth and fifth parts present the original emulation approach that has been developed and implemented along the thesis work. The FPGA hardware implementation is described and the global procedure is presented. Clearly this chapter is more than important in the presented work! The proposed approach is original and very complex: original because there is no previous work on the design impact of SEU and very complex because the configuration bit assignment is kept secret by the FPGA vendors.

Chapter 5 is dedicated to the presentation of the whole bench of results obtained from the above experimental procedure that has been implemented into the FPGA hardware. The procedure has been repeated for 12 different benchmarks which have been selected according to their size to fit in the used FPGA. They have been tested with and without parity predictors. Many statistics have been derived providing an extremely valuable information about the FPGA resources sensitivity. The chapter also describes some interesting variations observed in the measurements that could be an additional topic of investigation. The results presented here are of very high interest for the reliability community. However, a question arises concerning the universality of the results: are the results valid for other FPGAs or is it necessary to redo the whole experiment. In this last chapter, a discussion about the generic information resulting from the work and its impact on the reliability strategies for FPGA would have been appreciated.

In conclusion, the proposed strategy was innovative and challenging because of the inherent lack of important information. The thesis works is ending with many important results coming from this interesting and original approach. I really appreciated the different aspects of the work as well as the deepness of the study. Globally, the results have been published in world-class symposia and conferences and so, the results have been recognized by the international community. For these different reasons, I give a very positive assessment on the whole quality and I am clearly in favor of giving to Mr Kvasnicka the degree of Doctor.
REPORT ON THE DISSERTATION:
Reliability Analysis of SRAM-based Field-Programmable Gate Arrays
by Jiří Kvasnička

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This PhD thesis deals with bit error effects, namely soft effects like Single Event Upset, in the configuration memory of SRAM-based FPGA that may alter the design implemented in the FPGA. Since FPGA become very popular and frequently used, especially in the prototyping, and they are used in diverse high-reliability applications, SEU mitigation methods are demanded. Lack of FPGA structure description and the bitstream information are the main limiting factors in the development of error detection algorithms and reliable FPGA design approaches. Fault models that would better reflect the influence of bit errors present in the configuration memory are necessary for reliability analysis of FPGA. Moreover, errors in an unused part of the configuration memory will have no effect, and those should be somehow classified.

Jiří Kvasnička addresses most of those issues in a well written thesis, where an extensive analysis of relation between bit error effects and different fault classes and FPGA resources is presented.

The dissertation consists of six chapters, and three appendix sections are attached. After the introduction that describes the motivation behind the work, in Chapter 2 and Chapter 3, the theoretical background on FPGA, soft error mechanisms and radiation as well as state-of-the-art methods of soft error mitigation are presented. The major part of the proposed approach and obtained statistical results is described in Chapter 4 and Chapter 5. Chapter 6 summarizes the achieved results, and topics of future interest in the respective field are drawn here. There are three appendices, containing a detailed description of the bitstream of the used HW and test results, attached to the dissertation.

There are 79 references cited in the thesis. Four reviewed and seven other relevant publications, as well as 13 remaining publications are stated by the author. Although the total number of author's papers is above-average, only a few relevant publications went through a review process. Moreover, the relevant publications are not very recent. Some of the remaining publications are, however, sort of non-accessible or internal reports and their listing in the references is rather questionable.

The main aim of the dissertation is to overcome some of the limitations associated with development and implementation of error detection methods (with focus on soft errors) in SRAM-based FPGA towards their reliability enhancement. These limitations were nicely summarized in the motivation section. Then, four main problems representing the objectives of the dissertation were stated.

After giving the theoretical background and analyzing the state-of-the-art methods of SEU mitigation and SEU impact analysis, Jiří describes the proposed approach that is based on precise FPGA fault classification. He defines four main fault classes and relates those to possible locations in terms of FPGA resources. For this purpose, models of main FPGA-related faults are created. Establishment of this platform helps to develop the bitstream error effect prediction method that uses graph representation of the FPGA resources. Hardware emulator for soft error
emulation in the configuration memory through the fault injection and consequent exhaustive test of a dynamically reconfigured FPGA benchmark was developed. Finally, SEU manifestation in several FPGA benchmarks is investigated, and interesting results and statistics are presented. The number of useful findings were reported.

Main contributions

The main contributions of the dissertation to both the respective science field as well as the relevant practical applications can be summarized as follows:

- Definition of new fault models related to single bit error in the configuration memory and error effects with respect to a particular design implemented in FPGA.
- Development of a new method for estimation of the number of sensitive bits that is based on the prediction algorithm selecting the harmless bits.
- Development and implementation of HW emulator platform in the SoC that enables the evaluation of SEU effects inside the FPGA by dynamic reconfiguration of a few FPGA resources or by single-bit alternation.
- Experimental results obtained through analysis of soft error affects on the implemented FPGA benchmarks show several interesting and useful statistics sorted by fault classes and FPGA resources, which might be helpful to FPGA users and even vendors, mainly from the reliability point of view.
- The reported guidelines, findings and outcomes may open new issues and stimulate further activities in the field.

Remarks, Comments and Suggestions

Formal imperfections:
- there are several typos and misspellings, e.g. "Smplified", "notes" --> nodes (p. 21), "build-in" (p. 31), "ollowing" (p. 83), "1MEV" --> 1 MeV (p. 19);
- also several grammar mistakes, e.g. incorrectly placed articles, missing articles, missing commas after "Therefore", "Generally", "However"; extra commas before "than", "that", "nor", "or"; use of "wasn't" (p. 39), "isn't" (p. 45), "doesn't" (p. 10); missing dot at the end of sentences (p. 4, 11, 42); "at figure" --> in Figure (pages 67, 76); improper word order, etc.
- table captions should be placed above the respective tables
- wrong definition of abbreviation: Not Self-Testing (NFS --> NST) - p. 41
- abbreviations FS and ST are explained one page later than first appeared (pages 40, 41)
- term "NP-hard" is not explained (p. 10)
- there should be a space between parameter values and units, e.g. 10 MeV (p. 19)
- µm unit is misstated for energy (p. 20)
- Joul to electron volt conversion should be: 1 J = 1,602 176 487 x 10^-19 eV (p. 15)
- "drain" is rather used than "collector" for a MOS device (p. 21)
- a 6-line long figure caption is quite unusual (Figure 2.7, p. 21)
- "fault-security" is mixed-up with "fail-safe" (pages 40, 41), it should be unified
- incorrect reference of Figure 5.3 and Figure 5.4 in the text (p. 67)
- Table 5.2 is not referred in text (table 5.1 is referred instead, p. 67)

Technical remarks, suggestions:
- HDL does not represent "a design level" (as indicated on page 11: "At a HDL level...") --> it could be RTL or higher in this case.
- Sentence: "The static functional effect means that it does not affect the function of the design, but the timing parameter of the design" (p. 44) contains contradictory statements and it was probably meant otherwise.
- The author should clearly distinguish between terms "faults" and "errors".
Questions

1. Is it or is it not too demanding, in your approach, to require the transistor level structure (even transistors’ sizes) of the FPGA under test for fault prediction? Could you comment that?

2. What can be still done, in order to use the proposed approach, if the FPGA structure is not available?

3. What was used as the reference benchmark (Fig. 4.13) in the proposed HW emulator of SEU? How is it guaranteed that the reference FPGA is fault-free?

4. How the A fault class should be treated? Could you give any suggestion?

Conclusion and evaluation

I appreciated the clarity of the dissertation, the well motivated fault classification and fault modeling carried out, the proposed fault effect prediction SW method and the developed HW emulator as well as the comparison of results obtained by SW and HW techniques. Hence, I can claim that Jiří Kvasnička met the objectives of this thesis and demonstrated a wide-range research potential and good practical skills.

Thus, I recommend the acceptance of this dissertation and support unconditional admission of Jiří Kvasnička to defend the doctoral thesis.

Bratislava, December 11, 2013

Viera Stopjaková
Review of Ph.D. thesis

Author: Ing. Jiří Kvasnička

Title of the thesis: Reliability Analysis of SRAM-based Field-Programable Gate Arrays

University: Czech technical university in Prague, faculty of information technology and engineering

The topic of the thesis is a methodology of reliability analysis of a SoC system which is implemented using FPGA. Namely bit error effects in the configuration memory of FPGA, namely those induced by SEU faults, are taken into account. The thesis brings two methods of evaluation of the bit error effects. At the first SW based SEU fault effect prediction that assumes knowledge of FPGA architecture and knowledge of bitstream associations to the FPGA resources. At the second HW emulator, that emulates soft errors in the configuration memory and classifies the fault effect. An evaluation with respect to the prescribed CVUT/FIT template follows:

1/ The current state of the art in the area corresponding to the thesis

The theme of methods, architectures and algorithms aimed to evaluate and to improve reliability and dependability of electronic devices is a subject of scientific research worldwide. The thesis contributes to the state of the art, namely in the area of modern electronic technologies, especially FPGA.

2/ Formal structure of the thesis

The thesis is structured as follows: In the chapter 2 basic terms and models from the area of FPGA architectures and their radiation sensitivity are explained in the context of reliability requirements. Chapter 3 brings a qualified overview of the state of the art including previous results and related works. Chapter 4 presents an overview of the author’s approach, namely the above mentioned two methods of the bit error effects evaluation are explained. The fifth chapter contains a survey of obtained results with bit errors effects analysis and/or emulation. Chapter 6 contains conclusion and assumed directions of a future work.

The formal level of the thesis is very good. There are very little formal mistakes excluding part 2.3. (Radiation) where some expressions should be explained or repaired, e.g.:

- Part 2.3.1., line 5: $1\text{eV} = 1.6 \ldots \text{eV}$ ??
- Part 2.3.2.3., line 6: The energy needed ... is $1\mu\text{m}$. ??
- Part 2.3.3., line 5 and others: ... dose of $0.48 \text{mSv a}^{-1}$. ?? (physical unit has not been explained)

3/ Satisfaction of the thesis goals

The thesis brings new ideas and practically usable scientific knowledge. Unfortunately the thesis goals are not explicitly declared within the text of the thesis. But from the part 1.2. (Problem Statement) it is possible to derive the main goal of the thesis as to evaluate an influence of bit errors in the SRAM-based FPGA configuration memory and to compare this
influence with another design (i.e. not FPGA-based) possibilities. This goal of the thesis can be considered as appropriately satisfied.

4/ Evaluation of methods used within the Thesis

From the scientific methodology point of view it is necessary to appreciate the development of two methods how to solve the declared problem, i.e. how to evaluate an influence of SEU faults which are attacking the SRAM-based FPGA configuration memory. These methods are of quite various nature (analytical versus experimental), so it is possible to verify both of them when used for the same case.

On the other side in the chapter 5, which describes some experiments and results of SEU emulation should be a part (somewhere at the beginning, say as a separate subsection 5.1), which concerns the proposed experiments methodology, experimental environment and single experiments setup. I recommend to insert this issue (briefly) into the presentation.

5/ Results and outcomes with new information

The main contribution of the thesis is a critical evaluation of the soft (SEU) faults influence for the FPGA circuits design and functionality. The thesis contains two developed methods how to evaluate an influence of SEU faults which attack the FPGA configuration memory. The first method is purely analytic, it enables to analyze step by step and influence of an error value of single configuration bits. Valuable are namely the developed fault models (part 4.3.) that enable to follow how the fault spreads within the FPGA structure. The second method uses HW based fault injection into a selected configuration bit. The methods can be used independently, so the results can be cross-checked (and - moreover - the developed methods can be verified).

6/ Critical notes, remarks and questions for the defence

- Due to the fact, that the goals of the thesis were not explicitly defined and critically evaluated within the text, it should be done during the thesis defence.
- Because there are some inconsistencies in the section 2.3. concerning radiation, I recommend to explain briefly the radiation variables and physical units (especially the flux and the dose variables and units, their connection, what it is the unit [msV a⁻¹] used in the part 2.3.3., etc.).
- Within the thesis, some simplifying assumption concerning the target FPGA structure were used (e.g. part 2.2.1 - only island-style of Atmel FPSLIC FPGA architecture is assumed). Is it possible to estimate a “generality level” of the developed methods and the conclusions derived from the methods utilization?

7/ Overall evaluation – an overview

The thesis reflects state of the arts in the given area of computer science and it brings new results and outcomes in the form of usable tools and valuable publications. The submitted thesis fulfills the requirements for a Ph.D. scientific work and general requirements stated by the law 111/1998 Sb. to award the Ph.D. title. I recommend this work for the Ph.D. defence.

Plzeň, 2.12.2013

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