Review of the Dissertation
"Programmable and Customizable Hardware Accelerators for Self-adaptive Virtual Processors in FPGA"
by Jaroslav Sýkora

Topic and Relevance
In his thesis Mr. Sýkora addresses the problem of specifying and implementing hardware accelerators for adaptive processors. The constantly increasing mask costs for new technology nodes make it highly desirable that future processor architectures will offer the possibility to be customized to the needs of different applications. Thus, the topic of the thesis is highly actual and research is needed to clear many questions in this regard.

Formal structure and organization of the dissertation
The thesis consist of five parts: Introduction, static scheduling approaches, dataflow at gate level, dataflow at chip level and an evaluation/conclusion. The introduction sets the scene for the thesis, describes the objectives and the state of the art with respect to the objectives. This part could have been much more elaborate and I'm missing a clear structure in the discussion of related work. It is very hard to follow the unstructured enumeration of published approaches without knowing in what respect it is related to the thesis. Also, the introductory part contains a chapter on technological aspects. This is mainly to motivate the need for latency tolerance at various abstraction levels in the architecture/microarchitecture.

Although the objectives are clearly stated, it is not clear, what target technologies are taken into account. Also, the objectives seem to be chosen somewhat arbitrarily. It would have been much better if they were all stated as a consequence of a more general goal.

Completion of the dissertation objectives
All three objectives are treated very thoroughly and the thesis clearly presents solutions for each of the chosen problems. Chapters 3, 4 and 5 describe the structure of a particular FPGA based HW accelerator, its problem and a solution to overcome this problem (partially). Chapters 6 and 7 introduce a new method to describe HW accelerators on a higher abstraction level while maintaining a high degree of parallelism in the description. Chapters 8 and 9 describe an extension of the existing microthreaded LEON3 implementation.
such that it can execute predefined microthreads in HW accelerators. The results of all three objectives are evaluated jointly in chapters 10 and 11.

Assessment of the methods used in the dissertation

In most cases, the thesis follows the well established evolutionary cycle:

- analysis of the current state → identification of the prevalent problems → proposal and implementation of alternatives/improvements → analysis of the new state

It occurs to me that in some cases more alternatives for the improvement could have been discussed. E.g. for the reduction of the instruction issue overhead very different solutions could have been investigated. Thus, in these cases one can not be sure about the quality of the solutions found.

Evaluation of the results and contributions of the dissertation

The results for the three main objectives vary strongly in their meaning and importance. The result regarding the ASVP improvement seems to me of minor importance, simply because there might be much better solutions than the one presented (although this solution already is a valuable improvement).

The results regarding the inclusion of HW accelerators into standardized microcontrollers are a bit ambivalent. On one hand the methodology is very interesting and solves many problems that are hard to overcome in non microthreaded microcontrollers. On the other hand, the plain performance of the UTLEON3 is disappointing and it could be argued that the speedups created by the implemented HW accelerators are not a consequence of the microthreading itself, but rather due to the inherent speed of the HW implementation.

Finally, the results regarding an improved specification of HW accelerators by means of the FTL description are very encouraging. This methodology certainly can have a great impact on future implementation practices. Unfortunately, the methodology, while being exercised on a real example, in its current state cannot be used by non specialist developers. It would have been desirable to give this aspect little more thought and attention. Mr. Sýkora obviously was aware of that fact himself, as he states in the outlook that a formal language for FTL would be needed to make general applicable.

Remarks, objections, notes, and questions for the defense

The thesis has several formal weaknesses. Many abbreviations are not introduced properly (e.g. at the point where they first appear in the text). Some examples for this:

- LFSR on page 8
- DFU and ASVP on page 17
- HWFAM on page 24

Several citations are not appropriate:

- AToTLfCS80: no type of publication given
- GbS: middle name of second author wrong, page 2006 certainly wrong (probably year 2006)
- AZW+02, GV03, HA99, HHM99, Hoa04, Kub04, Kub05, Men, OBDA11, TM05: No publisher, type of publication unclear
- NPKvL99: completely messed up
- REL03: conference name (book title respectively) messed up
- SAGPl2: No publisher, no page numbers, author names all capital letters

Some claims and expressions should be backed up by additional citations:
- page 4: why should heterogeneous architectures be better than homogeneous ones
- page 7: "Elastic Circuits"
- page 63: Why does DSP and image processing imply data driven operation?

Some cross references are incorrectly labeled:
- page 66: Sec. 6.2.7, 2. P: Erroneously referring to figure 6.1 (table 6.1 was meant).
- page 70, last P.: Again figure instead of the (correct) table.

Sometimes, expressions are used without properly explaining them or giving any information on the context:
- page 7: SELF protocol not put into context
- page 24: microthreading not explained
- page 74: macroplaces are not explained
- page 89, section 7.5.1: Exact meaning of pipe is not explained. Is it a pipe line_ or is it a simple connection?
- page 120: A very brief introduction into the meaning of the parameters „size 32x768“ would be required

In terms of the real content there are several comments given below:
- figure 1.2 suggests that this is a known fact. Either there should be a reference for this or it needs to be discussed.
- on page 47 in caption of figure 5.1, the author claims that 256 bit wide instructions are impractical. In an FPGA, this would require 8 BRams, which is not a problem at all.
- page 92, figure 7.14: A formal description of an FTL design is not explained. Do i have to draw something? Obviously not. Efficiency of design with FTL is not investigated. Eventually, on page 135 it is explained how FTL descriptions are written. This would belong here.
- In section 7.6.2, particularly in paragraph "Run-Time Performance", I would have expected to see a comparison with an optimized pipeline. Maybe, the GP-ASVP is simply very badly designed?
- page 102 in section 8.2, a better explanation of the thread creation process is required.
- page 109 in section „Virtual Families“: Not all processors tolerate uneven addresses for the instruction fetch. This is a peculiarity of the used LEON3/Sparc V7 architecture.
- page 114, in paragraph „Portable accelerators“: The claim is not justified at all. No example for this is given, no arguments, no discussion.
Page 118, last paragraph of section 9.2.1: The number of thread executions actually carried out in the processor depends on the speed relation between software and hardware execution. It is not simply A/B!

Page 157, last section: The claims made here are not backed by any previous discussion. Moreover, the problems described here have not been mentioned before! This is not appropriate for a conclusion.

Overall evaluation of the dissertation
The thesis discusses a wide spectrum of problems and gives interesting answers to some of the questions. The sheer amount of work done is impressive and the results definitely deserve my acknowledgement. Nevertheless, after reading the thesis very thoroughly, I have the impression that the individual parts of the thesis are not as closely related to each other as I would like it to see. In some of the objectives still many open questions remain. I would have preferred to see a more focused thesis which maybe drops one of the three objectives in order to dive deeper into the remaining two objectives.

Regardless of this criticism, the work conducted is a fine piece of research.

Recommendation Statement
The author of the dissertation proved the ability to conduct research and achieve scientific results. In accordance with par. 47, letter (4) of the Law Nr. 111/1998 (The Higher Education Act) I do recommend the thesis for the presentation and defense with the aim of receiving the Ph.D. degree.

Darmstadt, 24.2.2014

Christian Hochberger
Recommendation on the thesis of Jaroslav Sýkora entitled:

*Programmable and Customizable Hardware Accelerators for Self-Adaptive Virtual Processors in FPGA*

The following is my report on this thesis based on the suggested outline provided.

*Up-to-datedness of the dissertation.*
I find the thesis to totally relevant to modern computing systems. It provides a motivation, based on power for the adoption of algorithms implemented in reconfigurable hardware and goes on to investigate accelerators both using vector floating point hardware as well as using gate-level dataflow. In particular, I was very familiar with work undertaken with the accelerator connected to an innovative microthreaded processor.

*Formal structure and organization of the dissertation.*
The format of the thesis is concise and very well presented, I had no problems in finding my way around the thesis and its structure flowed naturally for someone versed in the state of the art. Indeed it was a pleasure to read.

*Completion of the dissertation objectives.*
All stated objectives were completed to my satisfaction. Indeed the scope of the thesis is very broad with more than the usual number of objectives set and achieved.

*Assessment of the methods used in the dissertation.*
The candidate uses a broad range of methods and tools to achieve his objectives. These range from standard design tools for the development of a variety of architectures in FPGAs and the software to drive those architectures, through to the use of formal methods to synthesis lower-level designs based on the use of synchronous Petri nets. The use of these tools demonstrates not only good research but an aptitude for quality engineering, in the exploration and selection of the most appropriate solutions to the problems encountered. This has clearly resulted from a significant amount of training, a significant amount of background reading and an excellent aptitude for design.
Evaluation of the results and contributions of the dissertation.
I was particularly impressed with the evaluation of the results and contributions in the thesis. This was thorough and balanced.

Remarks, objections, notes, and questions for the defense.
A number of remarks, comments and questions, which will probably be made in the defence have been added as notes to the pdf of the thesis. I am happy for these to be passed onto the candidate.

The overall evaluation of the dissertation.
Overall I was very impressed both by the knowledge the candidate has shown in presenting his thesis and his understanding of the issues and results. Clearly he has an good grasp of the background literature and of the technology, tools and appropriate architecture for achieving his goals. He has also set a broad range of objectives and achieved all of these, some of which with quite significant results. There are areas where further research could improve on these results but the scope and achievements are significant when compared to other PhD dissertations I have examined. I therefore have no hesitation in making the following statement:

The author of the dissertation has demonstrated an ability to conduct independent research and achieve significant scientific results. In accordance with par. 47, letter (4) of the Law Nr. 111/1998 (The Higher Education Act), I recommend the thesis for the presentation and defense with the aim of receiving the Ph.D. degree.

In Much Wenlock on 21/01/2014

Professor C. R. Jesshope
Doctoral Thesis Review

Programmable and Customizable Hardware Accelerators for Self-adaptive Virtual Processors in FPGA

Submitted by Ing. Jaroslav Sýkora

The thesis has been submitted to the Faculty of Information Technology, Czech Technical University in Prague in Ph.D. study programme Informatics.

Up-to-datedness of the dissertation

We can base the evaluation of up-to-datedness of the doctoral thesis (DT) on a number of criteria. Foremost of those is the increasing demand for HW accelerators in computational, measurement and management processes. Among the important aspects of these accelerators are their flexibility, performance, power consumption and if possible also the low production cost. The submitted work satisfies a significant portion of the requirements placed on the research and design of such HW accelerators. The chosen FPGA technological platform guarantees both flexibility and, under certain conditions, also the low production cost. The HW accelerator design methods used in the DT fully follow and enhance the latest trends in the field of research and design of programmable and customizable FPGA-based HW accelerators. The conclusions gained from the research can be generalized and used in the design of more complex parallel processor structures and systems.

Formal structure and organization of the thesis

The DT structure reflects the effort of the author to combine several partial themes into a compact product. The author for the most part succeeded in doing that, except for a few exceptions.

In the first two chapters the author presents his motivation for the research in the chosen field. He connects upon the current state of technology and the real-world requirements for the
design of HW accelerators. In these chapters he refers to a number of publications with research similar topics and tries, already in the introduction, to graphically present the thesis contributions in relations (Figure 1.4).

The splitting of the core of the DT into three thematic and one conclusion parts, achieved by the choice of sections, is logical, and stems from the three main areas of the DT's content:

Part I - Limits of Static Scheduling in Programmable Architectures,
Part II - Dataflow at the Gate Level,
Part III - Dataflow at the Chip Level.

Each of these parts contains two to three thematic chapters, which have a clear structure with a brief introduction, a proposed solution, an analysis, and a conclusion, where the author summarizes his contribution to the problem of the relevant research field.

The author starts the individual subchapters by briefly summarizing the current state of the art of the field, perhaps in too much detail and depth. That is the case of the Petri Nets in II Dataflow at the Gate Level. Furthermore, the author provides many technological details and experiment results of these technologies, without a clear connection to the principles of the proposed solutions.

Each chapter provides, in its conclusion, an evaluation of the performed research and the author's contribution.

In the last two chapters the author evaluates the success rate of the proposed architectures and once again summarizes his contributions in the individual fields of research.

Completion of the dissertation objectives

In chapter 1.3 Objectives and Contributions, the author lists four main objectives of the DT labeled as O1 to O4. All objectives are related to the research and design of Application Specific Vector Processor (ASVP)-based architectures. In addition to that, the objectives O3 and O4 also focus on the dynamically scheduled data-driven architecture for a general-purpose computing using microthreading. In this chapter the author also lists his five main contributions:

C1 Analysis of a statically scheduled instruction-driven vector processing architecture for a customized computing realized in a reconfigurable array.
C2 A method for achieving high-frequency instruction issue using dictionary tables in an architecture with wide horizontal instructions generated on the fly.
C3 Structured and extensible approach for synthesis of hardware controllers from synchronous Petri nets.
C4 A new technique for a dataflow hardware synthesis from Petri nets.
C5 Bridging the gap between the data-driven microthreaded procedural computation with the special-purpose data-driven hardware in reconfigurable arrays.

In Part I the author introduces the problem of statically scheduled vector processor (dataflow at the task level) where the implementation platform is an ASVP in FPGA. The contributions to this part are the contributions C1 and C2. Part II studies the issues of fine-grained dataflow using Petri nets. Contributions C3 and C4 are provided in this part. The Part III of the DT focuses on the chip-level dataflow. The author discusses the possibilities of connections of a highly parallel microthreaded multicore-capable processor to a specialized function hardware. Contribution C5 is attributed to this part.

Each part has a conclusion with a detailed recapitulation of all achieved results and contributions in the field. The stated goals of the DT are in a harmony with the achieved results.
Assessment of the methods used in the thesis

The methods used in the DT are mostly relevant to the research, design and implementation of the hardware accelerators. This includes the methods for testing of the designed devices and the analysis of the experimental results. To verify the success rate of the proposed devices the author uses, not entirely systematically, different test tasks in different sections. For example, in Part I he uses the methods of Matrix Multiplication (MATMUL), a Mandelbrot Fractal Set (MF-set), and Image Segmentation (ImgSeg) for accelerator performance measurements. In Part II he only uses the MF-set method, and in Part III the soft-core accelerators applied to Finite Impulse Response filter (FIR) and Discrete Cosine Transform (DCT). The author does not explain or justify his choice of case studies or test tasks. It would certainly be interesting if he compared his designs with their equivalents implemented in GPU-CPU architectures and of course in DSP.

The testing and evaluation methodology used in the DT is not entirely systematic and compact. For this reason it is my opinion that they cannot provide an objective comparison and evaluation of the DT's results with existing solutions.

Evaluation of the results and contributions of the thesis

The DT does not always provide a clear connection in between a suggested problem and the state of research of the problem's field. It is difficult to recognize which parts of the text are suggestions of the author and which parts were already solved in other works. The author performed a number of experiments on the accelerator architecture designs. But the success rate of his improvements can't be compared just to GP-ASVP (chapter 10.2). There is no comparison whatsoever to the CPU-GPU systems and DSP. The set of benchmark algorithms is also insufficient. From the general principles' perspective, which should be the focus of the DT, it is not important how a given particular solution performed in a certain circuit or a certain version of a device. A statistical shortcut which would generalize a given idea and allow its use in further research would much more useful. This is another reason why the wider spectrum of test cases and a comparison to competing technologies should be present in the DT.

In any case the goals of the DT were eventually achieved and the author himself supports his case in several places with great emphasis. It is sometimes difficult to resist such suggestive and repeated argumentation.

But it would still be more suitable if a thematic part were researched to such a depth that the conclusions and the generalized contribution of the author for that research field, and how his solutions are superior to the existing ones, were obvious to the reader - there's beauty in simplicity.

Remarks, objections, notes, and questions for the defense

The DT exhibits several formal issues in descriptions, but I won't go into those here. Some abbreviations are not defined, or are defined only after their first use in the text. Abbreviations used in figures, tables, and pseudocodes are often never explained (the author probably assumes their meaning is known to the reader).
Some references to the used literature are incomplete (e.g. in Kub04, Kub05 the publisher and the publication type is not provided). In the author's publications the author shares (X.1 to X.3, X.5, X.8, X.9, X.12) are not listed.

Questions:
- Would the author be able to add instances of some test cases used in his work as applied to CPU-GPU and DSP?
- Since the great majority of the author's publications has further co-authors, could the author provide their share on the contributions C1-C5?
- The author provides mostly a rather old literature of the Petri nets field. Are the results achieved by the improved specification of HW accelerators using of the FTL description really promising, and what is the author's share on this contribution?
- What is the effect of the memory architecture (L/S unit, bank number, latency etc.) on the performance of his proposed solutions? Does the optimal performance depend on the test cases?
- Could the author provide a performance comparison between his proposed solutions and CPU-GPU and DSP when measured by the test metrics used in chapter 10.2?
- A number of different tasks were used as case studies and test applications. Can the author explain and justify their choice?

Overall evaluation

I consider the DT successful, despite the critical remarks listed in the previous paragraphs. The reason for this claim lies in the amount of work that the author had to do to achieve the presented results. Despite its wide thematic spread and a great amount of text, the DT doesn't contain significant formal or factual deficiencies and is easily readable. It would be better to focus on one particular compact problem, research it into a greater depth and connect it precisely to existing solutions, and to better and more objectively test it – “less may sometimes be more”. If such were the case, it would be easier to express the generalized conclusions and contributions of the DT – and clearer to the reader.

Recommendation Statement

The author of the dissertation proved the ability to conduct research and achieve scientific results. In accordance with par. 47, letter (4) of the Law Nr. 111/1998 (The Higher Education Act) I do recommend the thesis for the presentation and defense with the aim of receiving the Ph.D. degree.

V Praze dne 28. 2. 2014.
Róbert Lórencz